Does FPGA-based prototyping really have to be this difficult?

Embedded Conference Finland

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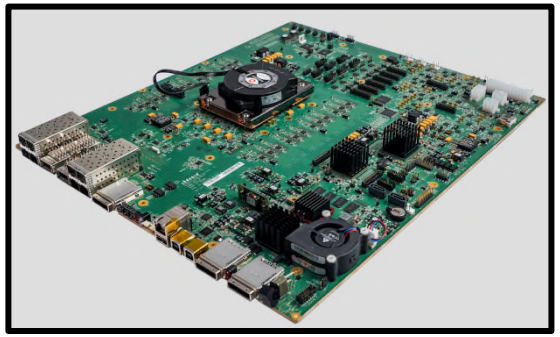
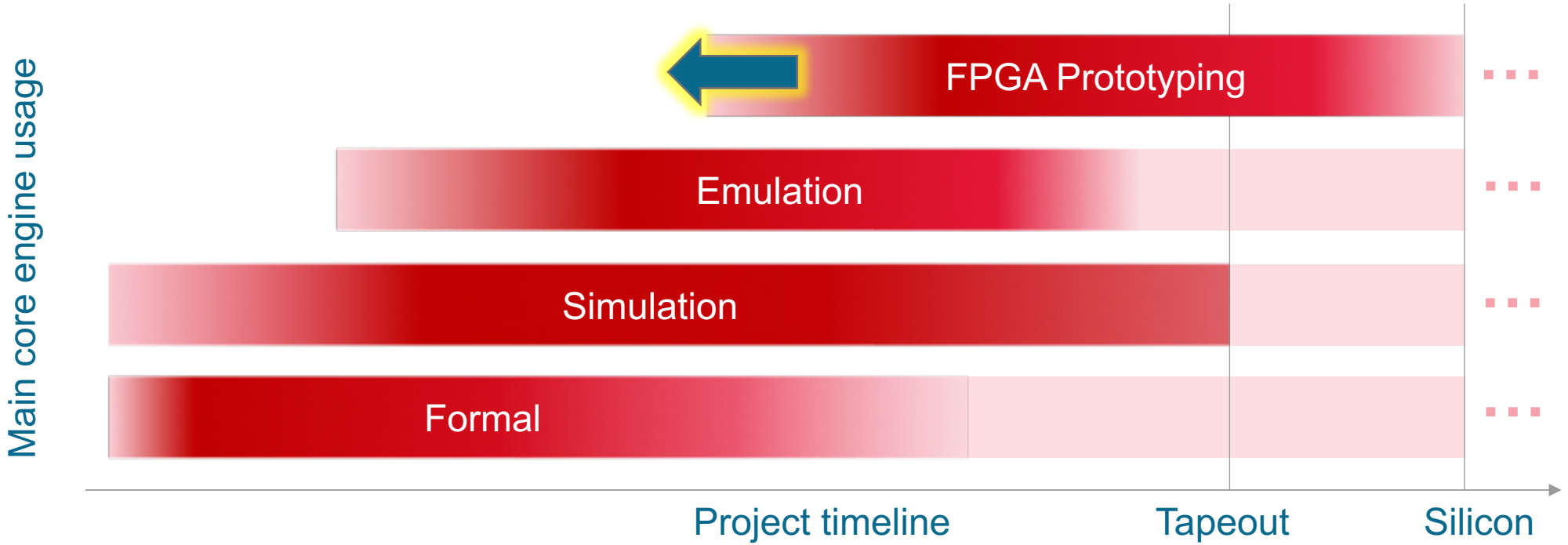
What is FPGA-Based Prototyping?

- **Primary platform for pre-silicon software development and validation**
  - Maps a digital ASIC, ASSP, SoC design or part thereof into one or more FPGAs
- **Allows SW to simulate in real world environments**
  - Provides pre-silicon execution speeds in MHz
  - Enables connectivity to real peripherals
    - Runs real world traffic flows including interrupts and unpredictable events
    - Runs error conditions and handling errata with other system components



FPGA-Based Prototyping as part of your verification solution

- **Ever-increasing verification** requirements driven by growing hardware and software **complexity**
- **Fast time to results** is essential to ensure projects can **meet schedules**
- **Right tools for the right job**: Combination of formal, simulation, emulation and FPGA prototyping



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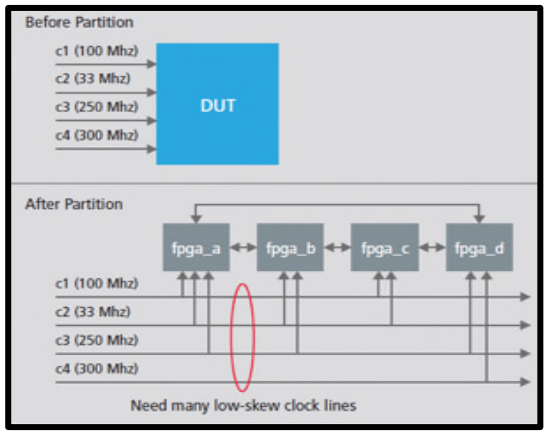
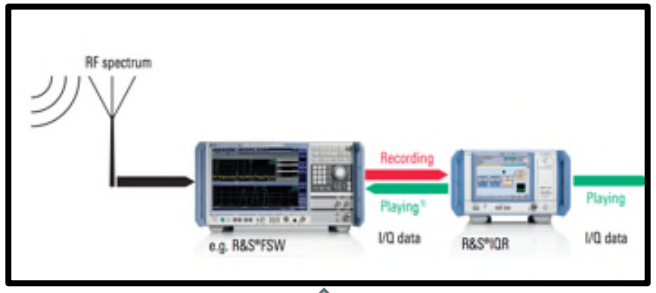
FPGA-based prototyping is hard to do

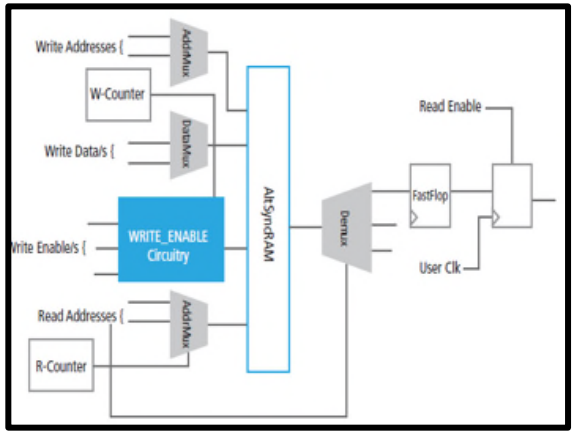
Clocking

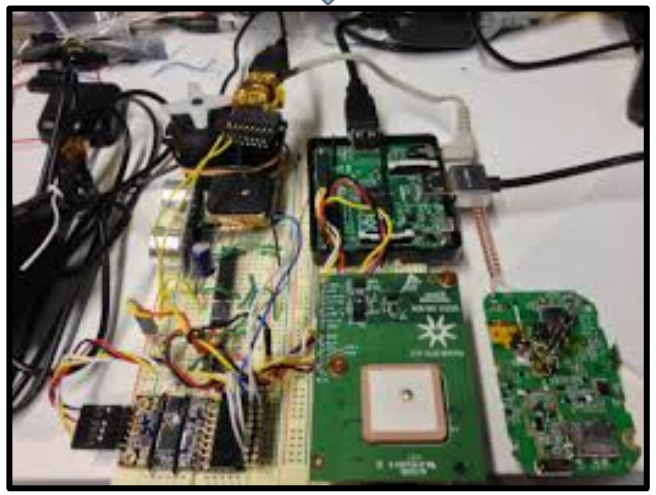


Interfaces

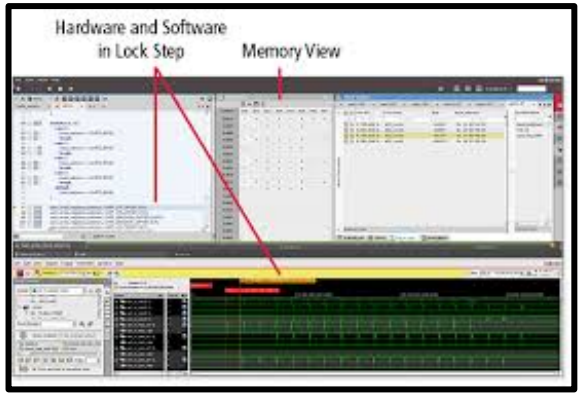


Memories

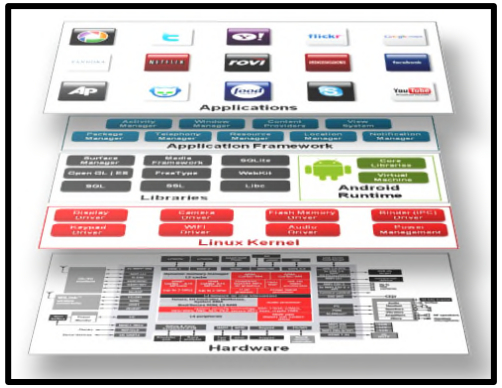




Debug



Software



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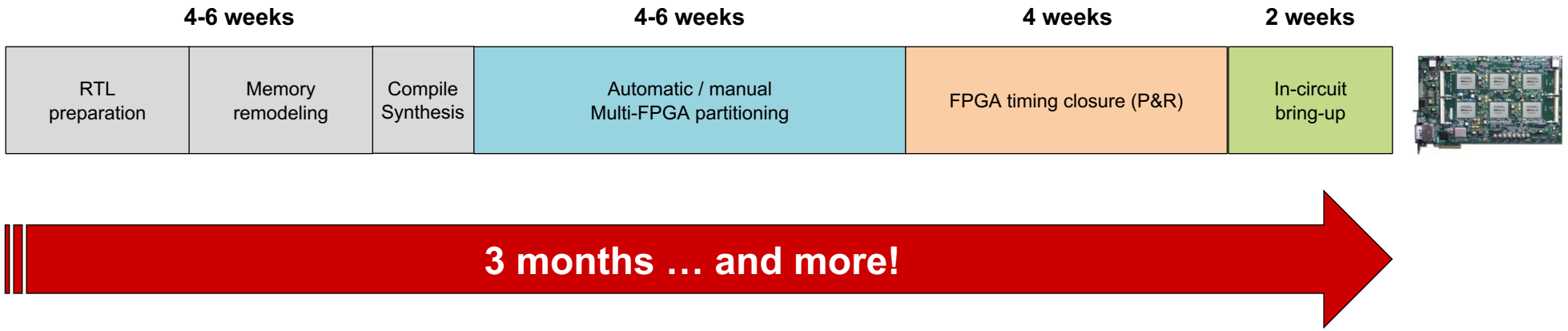
Really, really hard to do

FPGA-based prototyping has become the methodology of choice for early software development.

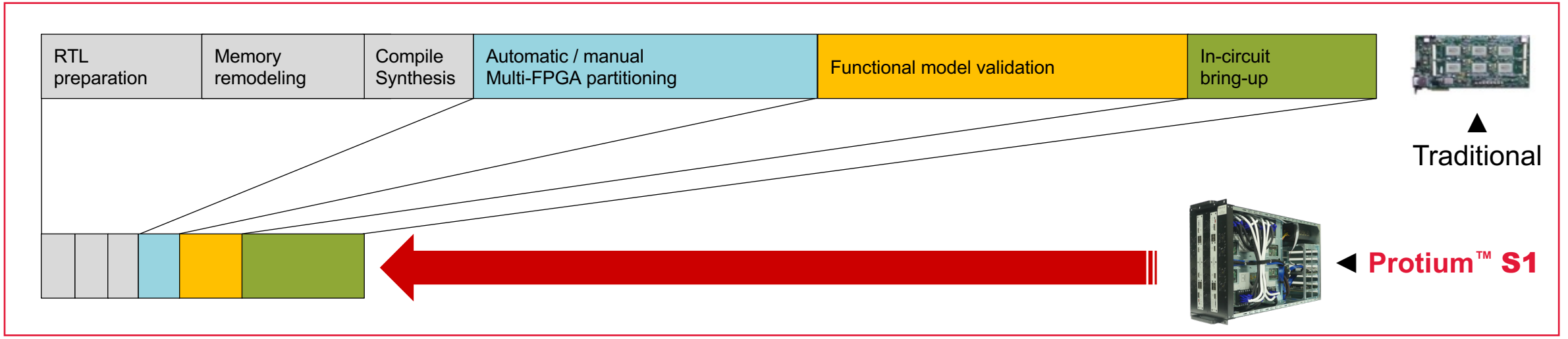
BUT …

Prototyping implementation and bring-up takes too long and there has, so far, not been any easy transition from simulation and emulation into FPGA-based prototyping.



Or is it?

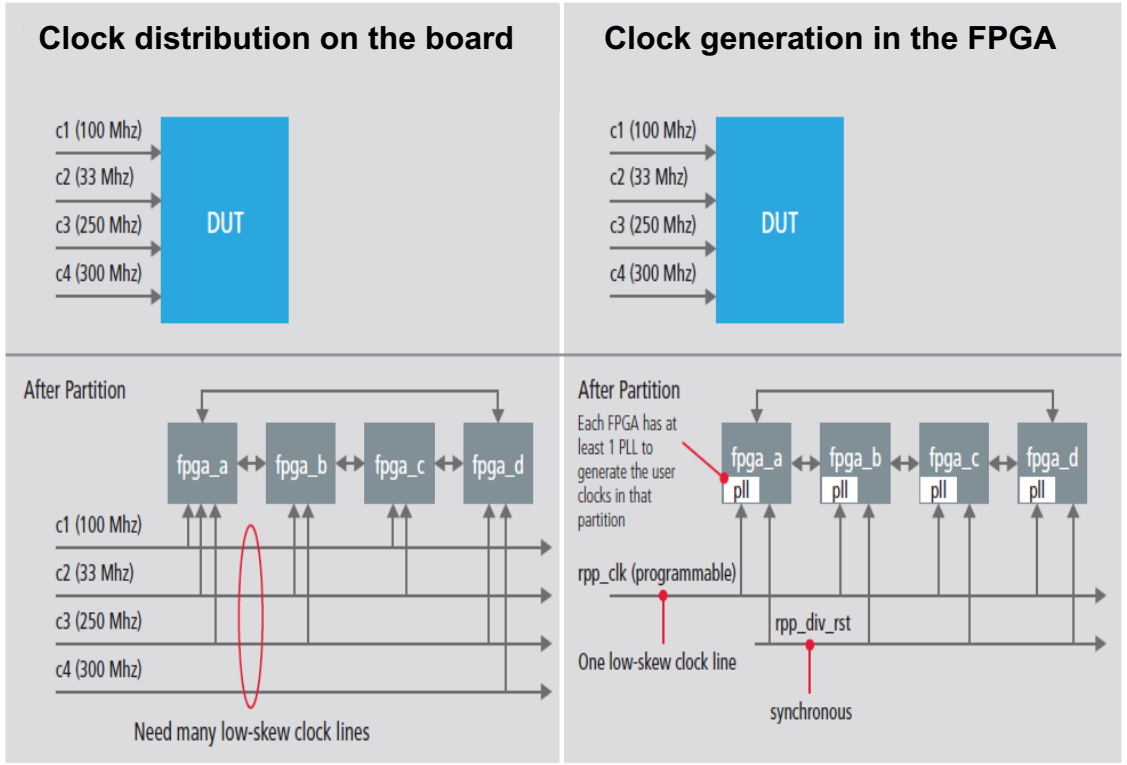
Protium S1 – Addressing the prototyping challenges



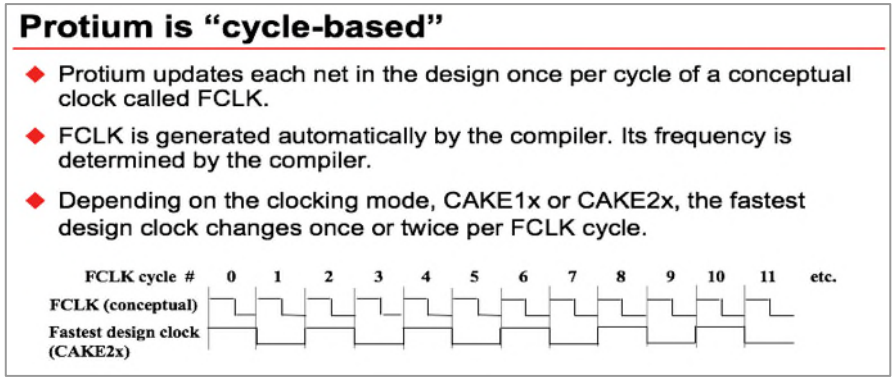
- No RTL modifications needed
  - Clocking / number of clocks
  - Automated memory compilation and modeling
- Fully automatic, multi-FPGA partitioning
  - Optional manual optimization
- Pre-FPGA P&R model validation
  - Multiple design integrations per day
  - Avoids time-consuming FPGA P&R
- Fully integrated FPGA P&R
  - Automatic constraint generation
  - Guaranteed P&R success

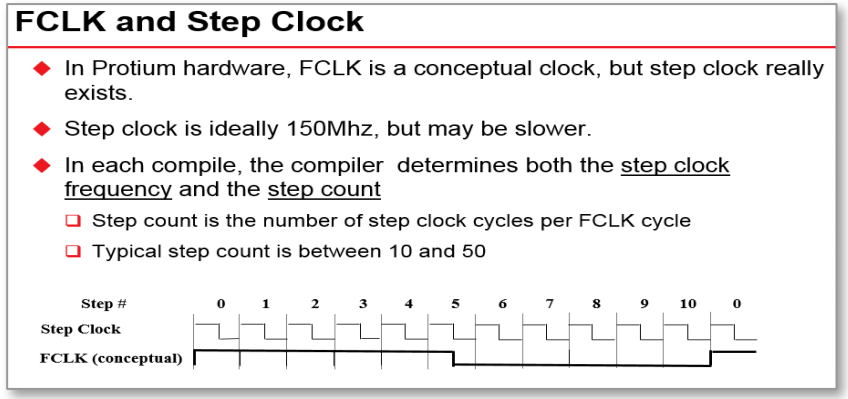
Advanced clocking – any type and number

- Traditional imitations:
  - Gated clock, multiplexed clocks
  - # of clocks
  - **Difficult to achieve FPGA timing closure**
  - **Long iteration times / long FPGA P&R times**
  - **Unpredictable results & prototype behavior**



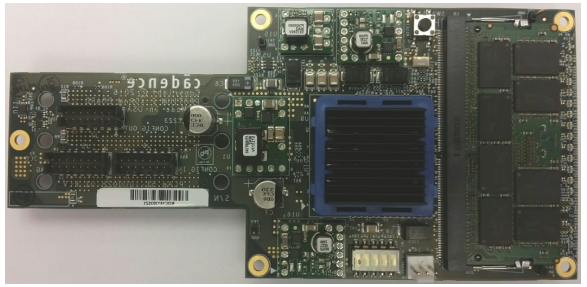
- Protium™ benefits:
  - No hold-time violations in user clock domains
  - Removes any FPGA-specific clock limitations
  - **Supports unlimited # of design clocks**
  - **Improves FPGA timing closure**
  - **Accelerates FPGA P&R times**

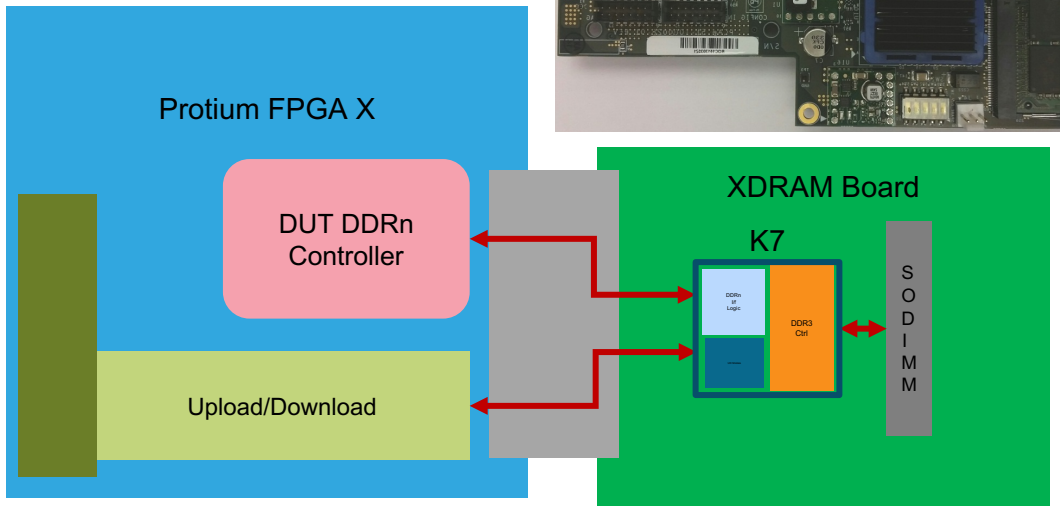




Comprehensive memory support

- FPGA built in & XSRAM
  - Benefits:
    - Automatic mapping of any memory type
    - Support for multi-port memories
    - Support for backdoor upload/download
  - XSRAM adds:
    - Increases FPGA internal memory from 80Mbits to 128MBytes
- XDRAM
  - Benefits:
    - Adds DDRx bulk memories
    - Supports LPDDR2/3/4; DDR3/4; HBM
    - No change to design memory controller and firmware
    - Support for backdoor upload/download
    - Acts as memory speed bridge (timing, refresh, etc.)

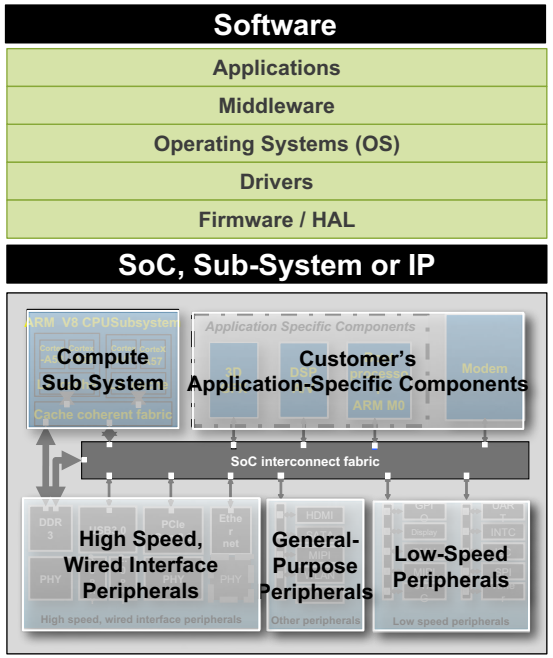




- Directly Connected or Full Custom
  - Daughter cards available for more custom approaches if required

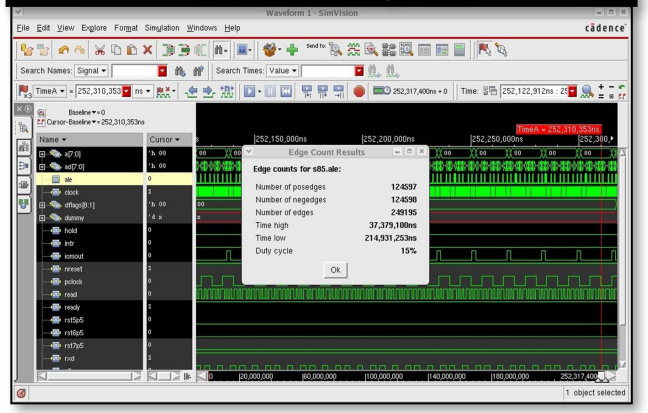
Hardware and software debug

- Waveforms across partitions
  - Design-centric view vs. FPGA-centric
- Force/release
  - Predefined signals (at compile time) to “0” or “1” during runtime
- Monitor signal
  - Real-time monitoring of predefined (at compile time) signals



- Backdoor memory access
  - Quickly change boot code, software, etc.
- Clock control
  - Start/stop the clock on demand
- Fully scriptable runtime environment
- Remote access
  - Network resource anytime from anywhere
- High-performance link to software model

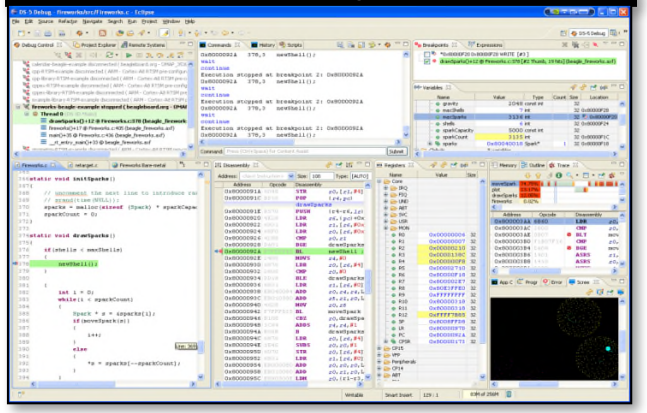
Hardware Debug: RTL



Probes

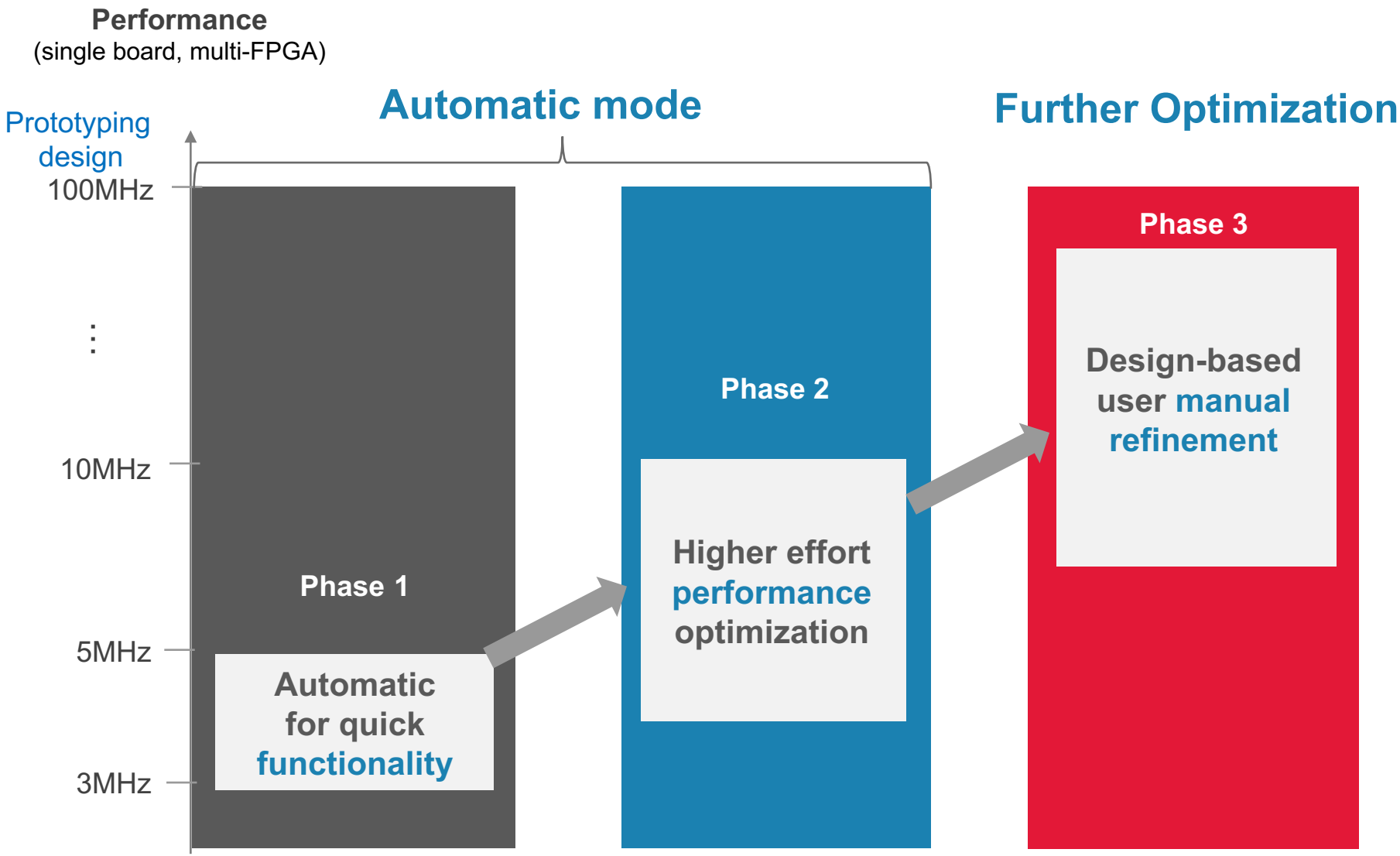
JTAG

Software Debug: C Code



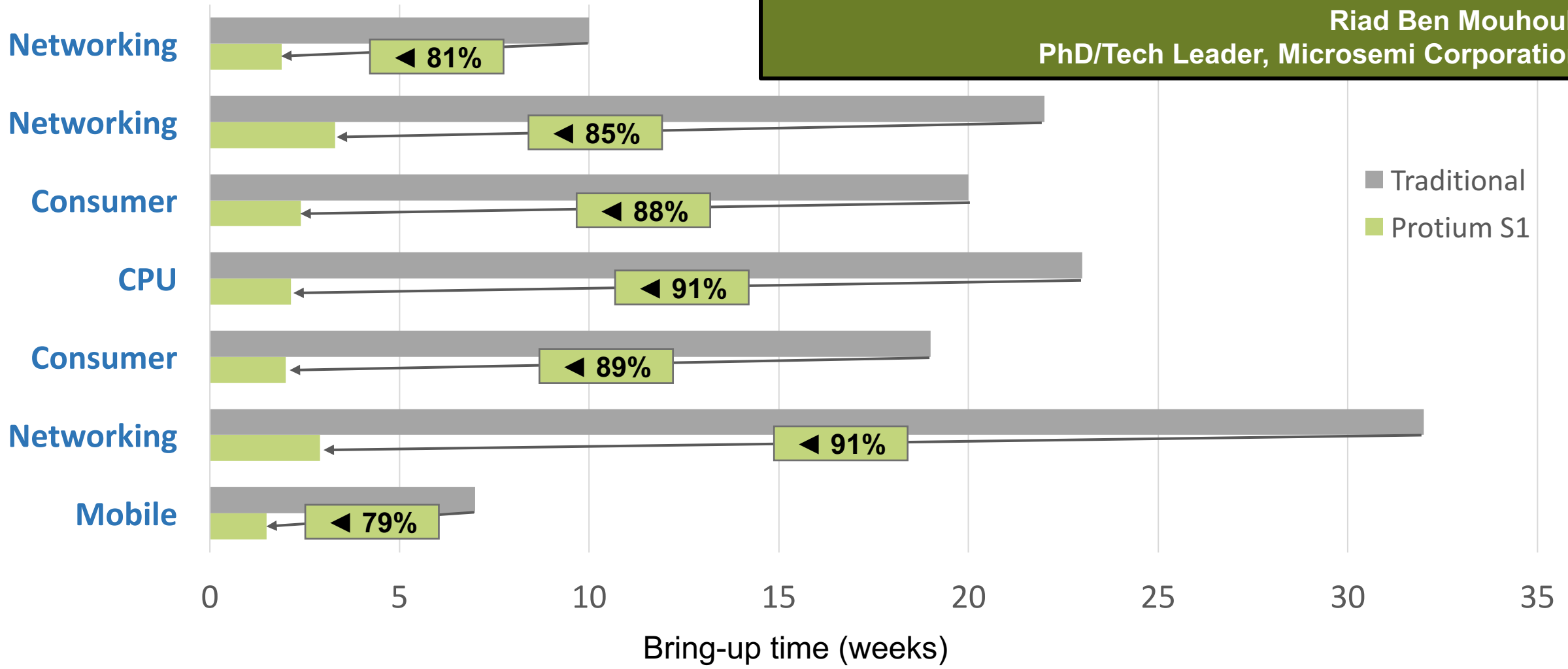
UART – to peripherals

Scalable performance



Fast Time-to-Prototype (TTP)

> ***"Protium™ has incredibly simplified our prototyping flow. It allowed us to significantly improve prototyping bring-up time."***
>
> **Riad Ben Mouhoub**
> **PhD/Tech Leader, Microsemi Corporation**



Note: Sample customer bring-up gains over traditional FPGA-based Prototyping solutions

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Microsemi @ CDNLive … challenges & requirements

- Mapping design to multiple FPGAs is not automated: design partitioning
- Clocking issues
- Manual interventions and several iterations for timing closure
- ASIC RTL modifications
- FPGA debug tools improved, but still not good enough to tac
  complexity
- Peripheral availability: daughter cards for PCIe, USB, DDR,
- Memory mapping
- Reusab… most of the time, custom platforms are not reus

Why explore new prototyping platforms?

The traditional FPGA-prototyping flow has
up, it is hard to debug, and its performanc
always what we expect.

Why Choose Protium ?

- Shares a common front-end flow with Palladium, which results in easier builds maintenance !
- Protium HW can be used with any custom flow
- Requires no ASIC RTL modifications
- Does not need manual intervention for timing closure
- Users can easily generate as many clocks as they need
- Large variety of peripherals and memories to quickly connect the DUT to a realistic environment
- Can use traditional on-chip debug tools or port the design back to Palladium
- Forces and monitors
- Memo… backdoor access for debug and quick FW deposits: compatible wi… Z1 scripts

– Protium has incredibly simplified our prototyping flow
– It allowed us to significantly improve prototyping bring-up time
– It helped to off-load Palladium and use it in a more efficient way

Microsemi

10

Power Matters.™

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… and this is what our customers are saying!

Amlogic @ DAC 2016

11 Why Palladium and Protium

- Run software exactly same way as real silicon
  - Compile, "flash" and run
  - Boot from SD card or eMMC/NAND
- Rich debug capability
  - JTAG & UART
  - Memory capture and restore
  - Stop clock and set/reset signals
  - Trace any signal on Palladium XP
  - Capture pre-defined signal for offline viewing on Protium

Amlogic

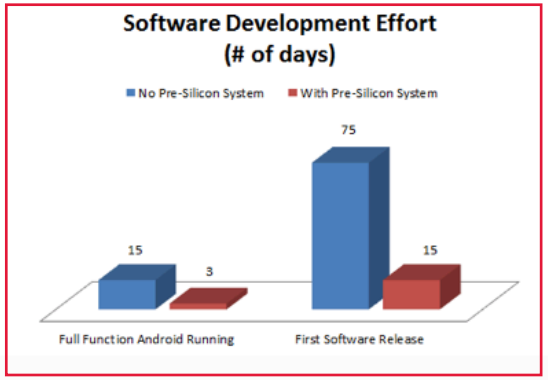
10 Why Palladium and Protium

- Quick design bring-up
  - No RTL modification
  - Palladium XP and Protium share same compilation flow
  - Available as early as RTL is ready
  - Complete pre-silicon platform
- Scalable and flexible
  - Scalable to accommodate future design
  - Flexible to run multiple small designs concurrently
- Good speed
  - 1MHz on Palladium XP
  - 5MHz on Protium in fully automatic mode (no manual guidance and optimization)

Amlogic

16 Results & Limitation

- Software is READY when silicon returns
  - Basic Android running in 30 minutes after silicon is back
  - Full Android demo to customer in 3 days
- Limitation
  - Analog module is not verified on emulation system
  - Digital-analog interface is not 100% same as real chip



Amlogic

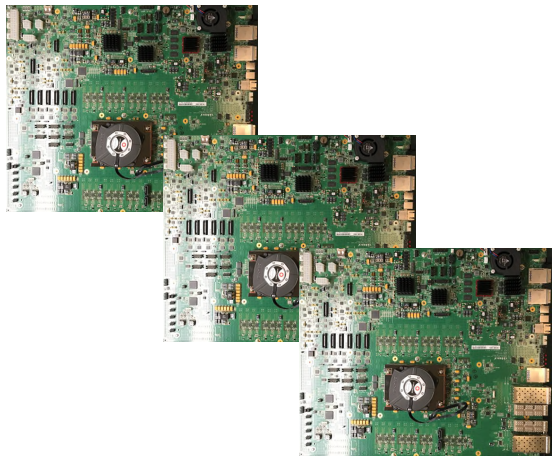
… and Xilinx likes it too

"The Cadence Protium S1 platform ensures scalability to hundreds of software developers at the earliest possible point during the development flow, and allows developers to focus on design validation and software development rather than prototype bring-up. The common flow with the Cadence Palladium Z1 emulation platform enables a smooth transition from emulation to prototyping, which greatly improves productivity."

-Peter Ryser, Senior Director for System Software, Integration, and Validation, Xilinx

Industry's most comprehensive hardware portfolio

Protium G1



Single board

- 1 FPGA
- Up to 25M ASIC gates
- Affordable and scalable
- Highest performance
- Early software development
- IP verification

Protium S1-SC

Single chassis system

- 2-8 FPGAs
- Up to 200M ASIC gates
- Flexible and scalable
- Fastest bring-up
- Unique SW debug capabilities
- Early software development
- HW/SW integration

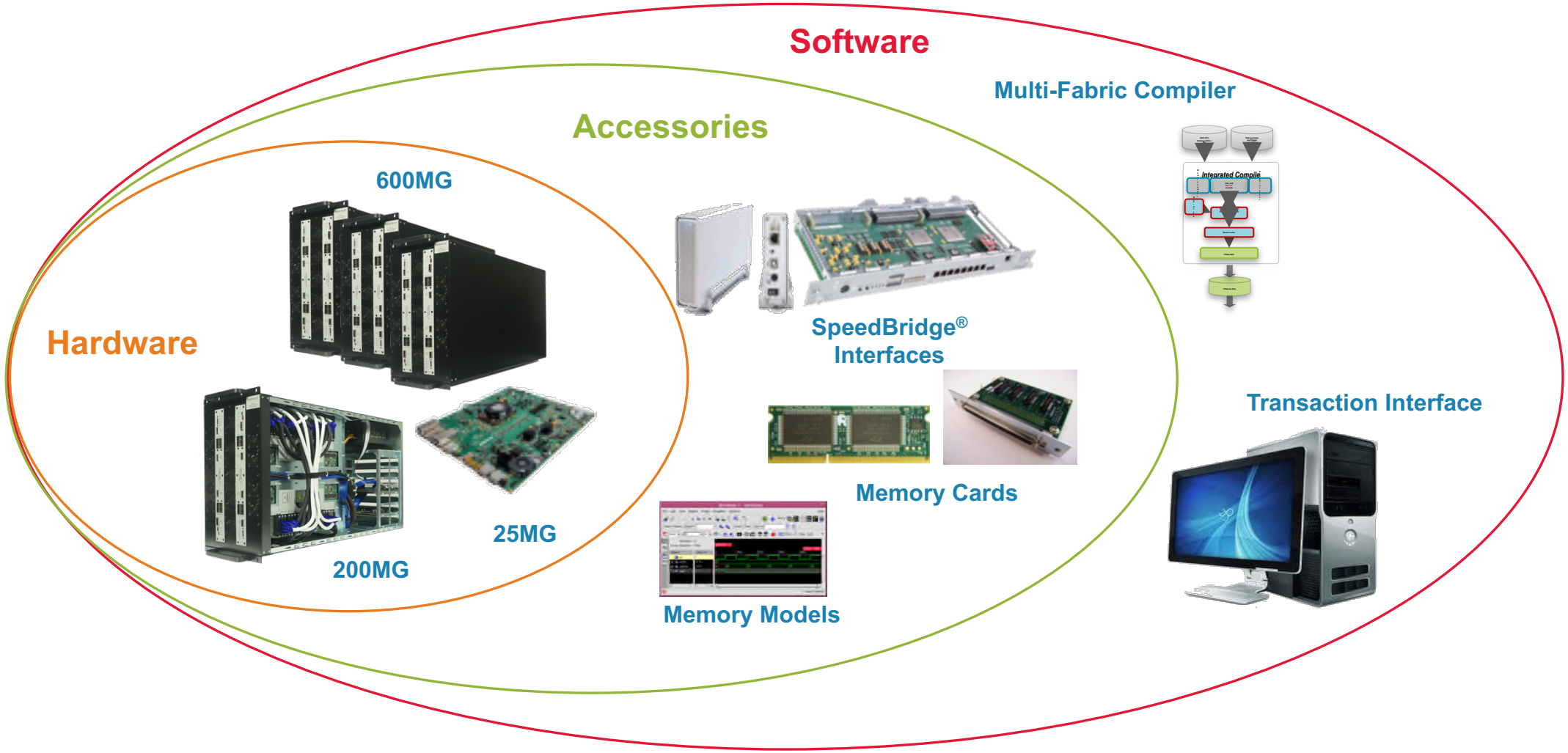
Protium S1-MC (2H 2017)

Multi-chassis configuration

- 8-24 FPGAs
- Up to 600M ASIC gates
- Highest capacity
- Flexible use modes
- Advanced debug
- High performance regression
- Full system validation

Protium S1 System and Environment

Comprehensive prototyping solution: High-performance and optimized



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Protium S1 – the Most Efficient Way to Prototype Your ASIC

- **Fast time-to-prototyping** (months down to weeks)
  - No RTL changes
  - Automatic partitioning/memory compilation
  - Fully integrated FPGA place-and-route
- **Scalable performance** (3-100MHz)
  - From fully automatic to fully manual
  - Advanced black-box methodology
- Advanced **software debug**
  - Memory upload/download
  - Force and release
  - SCE-MI transaction interface